StreamStor 10 Gigabit Ethernet Daughterboard

User Manual

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About This Manual

This manual is intended to serve the following purposes:

- to provide an overview of the StreamStor 10 Gigabit Ethernet (10GigE) daughterboard;
- to act as a reference for the operator;
- to provide guidance on software capabilities and choices and
- to provide the Declaration of Conformity documentation required for the CE Mark.

It is suggested that you periodically check the Conduant web site for the most recent software updates, application notes, and technical bulletins.

If you are unable to locate the information you need, please feel free to contact us by e-mail or phone.

Overview

The StreamStor 10 Gigabit Ethernet ("10GigE") daughterboard is a mezzanine IO board that can be used with a compatible StreamStor controller such as the Amazon or Amazon Express.

The Conduant StreamStor 10GigE recording system is a "formatless" Ethernet packet recorder for recording real-time data streams. The system generally includes a mezzanine (or daughter) board on a StreamStor recording controller along with storage media (disk drives). The system is intended to provide a means to use 10GigE hardware to transport real-time data streams for recording purposes. This may involve routers or other network equipment but, in general, the system is not intended to function as network interface nor does it provide any facilities to respond to standard network protocols or queries. In addition, it is left to the user to define the data contents and format of the recorded data. Each Ethernet packet that arrives at the interface is assumed to carry one data frame to be recorded. This document describes the contents and format of these data frames. The source hardware must create the data frames in this format for successful recording on the StreamStor system.

Ethernet Packet Format

Packet structures will adhere to standard IEEE 802.3 Ethernet packet specification. The general structure of an Ethernet packet is shown in the following diagram.

<table>
<tr><td></td><td>Preamble (8 bytes)</td></tr>
<tr><td></td><td>MAC Client Header
(14 bytes)</td></tr>
<tr><td rowspan="2">MAC Client Data</td><td>Upper OSI layer parameters
or other non-relevant data</td></tr>
<tr><td>Data Frame</td></tr>
<tr><td></td><td>Frame Check Sequence
(4 bytes)</td></tr>
</table>

The components of an Ethernet packet include:

- Preamble – a synchronization pattern that allows the Ethernet hardware to synchronize properly to the Ethernet packet.
- MAC Client Header – contains such information as Source and Destination MAC addresses and Ethernet type.
- MAC Client Data – this is the data that can be recorded depending on the Data Payload Offset value.
- Upper OSI layer parameters – such parameters as OSI Layer 3 IP and higher-layer parameters may be contained here; they are assumed to be of fixed length for a given recording.
- Data Frame – the data frame contains the source generated data including any header data; the user must specify the byte offset from the beginning of the MAC Client Data at which recording is to start ('Data Payload Offset'). This allows the user to decide whether to include or skip the OSI layer data and any header in the data payload.
- Frame Check Sequence (FCS) – a cyclic redundancy error-checking value that is only used to validate that a packet was received without error (not recorded).
- Within each recording session, all Ethernet packets should have exactly the same length and structure.

Data Frame Format

Each data frame must meet the following guidelines:

- Each Ethernet packet arriving at the recorder contains one data frame.
- Each Ethernet packet should have a constant-sized OSI layer data size.
- Any data not intended to be recorded must be at the beginning of the data frame, immediately following any OSI layer data, and can be of any size.
- The data to be recorded starts at a specified offset from the start of the MAC Client Data section (Data Payload Offset). If this offset is zero, everything in the MAC Client area, including any OSI layer data, is recorded. The offset can also be used to skip the recording of header data that is immediately following any OSI layer data.
- The data to be recorded in each packet must have a length that is an integral multiple of 8 bytes.

Data Format

The data, which immediately follows the MAC Client Header, is defined as the MAC Client Data. The MAC Client Data area of the packet may include OSI layer data. If the user does not intend to record the OSI layer data, then an offset (Data Payload Offset) must be supplied to the StreamStor controller to skip over it. This value is defined as the number of bytes counted from the start of the MAC Client Data. Note that this offset may also skip over any header or other data at the start of the Data Frame area. Also, it must also be provided to the StreamStor controller prior to the start of a recording and must remain fixed throughout that recording session.

The amount of data to be recorded from each packet received is determined by the difference between the MAC Client Data size and the user-provided Data Offset. The amount of data recorded from each packet must be a multiple of 8 bytes. StreamStor supports the use of jumbo Ethernet packets up to 9000 bytes.

Data Recording

Recorded Data

Once the recording has started, the StreamStor system will record a portion of all received packets, from the start of the Payload Data Offset to the end of the packet, exclusive of the CRC value. The Payload Data Offset value must be provided to the StreamStor recorder prior to the start of a recording. Note that a value of zero is a valid choice. An offset value of zero will allow the recording of the following for each packet: any OSI layer data, the data frame header and the payload data.

Packet Order

Due to the nature of Ethernet hardware and network design, it is possible for packets to arrive at the recorder out of order. In point-to-point implementations, this ordering problem cannot occur. However, if routers or other network equipment is utilized in the movement of data to the recorder, this ordering problem can occur. Packets must include sequence numbers within the data stream to allow the order to be corrected upon data retrieval. Otherwise, the StreamStor hardware can be adapted to provide a minimal amount of re-ordering capability, if required.

Raw Mode

The StreamStor hardware supports a “raw” mode to record complete Ethernet packets for testing purposes. This includes the entire contents of the packet, as defined earlier, with the exception of the Preamble and MAC Client Header. Packets that do not conform to the modulo 8-byte size restriction will be padded at the end of the packet to inflate the size to modulo 8. Contact Conduant engineering for more information on this mode of operation.

Packet Filtering

In some environments, it may not be possible to prevent Ethernet packets from arriving at the recorder that are not intended for the recording. The StreamStor hardware can be programmed to filter packets based on the source MAC address or the size of the MAC Client Data section. This filtering mode must be enabled in the StreamStor programming interface and the source MAC address and/or length to filter must be provided.

Performance

Depending on the StreamStor system being used the recording rate may not match that of the 10 GigE interface. Therefore, the source data stream must be adjusted accordingly to avoid continuous saturation of the interface and resultant packet loss. The maximum recording data rate is 500 MB/s for Amazon-based systems and up to 800 MB/s for Amazon Express-based systems depending on disk resources used. The Amazon controller can buffer up to 1 GB while the Amazon Express can buffer up to 2 GB of data. Either controller's RAM buffer can offload from the interface hardware at approximately 800 MB/s. The 10 Gigabit Ethernet interface hardware is capable of buffering up to 5 jumbo packets which is approximately 45,000 bytes.

Physical Layer

Media

The StreamStor recorder follows the 10GBASE-CX4 (802.3ak-2004) standard for interconnection with data sources. It uses the XAUI 4-lane copper cabling which is similar to that used by InfiniBand technology. It is specified to work up at a distance of up to 3m (~10 ft). Each of the 4 lanes run at the standard 3.125 Gbps.

Connector

The cable connection to the StreamStor recorder is a standard CX4 design with screws for a secure connection. Since the latch-style connector is more prevalent, Conduant offers a CX4 cable with a screw-style connector at one end and a latch-style connector at the opposite end.

Programming

Configuring 10GigE with XLRSetMode

The StreamStor API function `XLRSetMode` is used to set the input path and functionality of the StreamStor. Table 1 lists the supported modes.

TABLE 1 – 10GigE I/O Modes	
XLRSetMode Mode	**Description**
`SS_MODE_SINGLE_CHANNEL`	Receives and sends data over one channel

Setting up Channels

The StreamStor system can be configured to perform the following operations:

- record from the 10GigeE port or
- record over the PCI bus or
- playback over the PCI bus.

The port and the PCI bus are each mapped to a specific channel number, as shown in Table 2.

TABLE 2 – Channel Mapping	
Channel Number	**Channel Description**
0	PCI
28	10GigE Port

The 10GigE daughterboard supports recording a single channel. Multi-channel recording over the 10GigE port is not supported.

Input and output channels must be "selected" and "bound" before your application can record or playback data. The API function `XLRSelectChannel` is used to select a channel. When you select a channel, subsequent channel-specific API calls will be performed on that channel.

The API functions `XLRBindInputChannel` and `XLRBindOutputChannel` are used to identify which channel(s) will be used for data input and which channel(s) will be used for output. Playback over the 10GigE port is not yet supported.

The StreamStor SDK User's Guide describes each of the above API commands. The chapter called "Channel Description and Selection" provides an overview on using channels.

Single Channel Operation

By default, the 10 GigE daughterboard is in single channel mode. You can explicitly set the mode to single channel by calling `XLRSetMode` with the mode parameter set to `SS_MODE_SINGLE_CHANNEL`.

When in `SS_MODE_SINGLE_CHANNEL` mode, the default binding for channel input and channel output is the PCI bus (channel 0). To change the binding, call `XLRSelectChannel` and `XLRBindInputChannel` and/or `XLRBindOutputChannel`.

The following code fragment shows the sequence of API calls to use if you want to record over the 10GigE port (channel 28).

```
XLRSetMode(xlrHandle, SS_MODE_SINGLE_CHANNEL);
XLRClearChannels (xlrHandle);
XLRBindInputChannel(xlrHandle, 28);
XLRSelect (xlrHandle, 28);
XLRecord(xlrHandle, 0, 1);
   … record for a while …
XLRStop(xlrHandle);
```

It is important to note the order of the API calls. The `XLRSelectChannel` command selects the channel that subsequent API commands will act upon.

Programming Ethernet Registers

The 10 Gigabit Ethernet Daughterboard has requirements based on Ethernet Filtering and metrics. This section discusses how to use the Ethernet Filter Registers.

Ethernet Filter Control Register

The Ethernet Filter has its own set of registers which can be used to enable/disable raw mode, CRC checking, and to set promiscuous mode.

To configure the 10GigE daughterboard's Ethernet Filter, call the StreamStor API function `XLRWriteDBReg32`. The function prototype is:

```
XLR_RETURN_CODE XLRReadDBReg32( SSHANDLE device, int
Register, OUT UINT32 Value );
```

Where:

- device – the StreamStor handle
- Register – the index of the register to write
- Value – the value to write

The register index for the Ethernet Filter is #defined as:

```
SS_10GIGE_REG_ETHR_FILTER_CTRL
```

The 10GigE register indexes are described in Table 3. They are defined in the StreamStor header file `10GigeRegs.h`. We recommend that you use the identifier instead of the actual index in calls to `XLRWriteDBReg32`. Doing so will obviate the need to change the values if the registers change in future releases and will make your code easier to read.

For example, to set the Ethernet Filter Control Register to a value:

```
XLRReadDBReg32(sshandle,SS_10GIGE_REG_ETHR_FILTER_CTRL,value)
```

Raw Mode

Bit 0 of the Ethernet Filter Control Register is used to set or clear "raw mode." Raw mode is useful for debugging packets.

If raw mode is enabled, the packets pass completely through with no filtering, including the MAC Client Header. If raw mode is enabled, all others modes are ignored.

CRC Disable

Bit 2 of the Ethernet Filter Control Register is used to enable/disable CRC ("cyclic redundancy check") checking. CRC checking is normally enabled, which means that all Ethernet Frames are checked for CRC (Fault Symptom Code).

When CRC checking is enabled (the default), a payload is not passed to the Filter if it contains a CRC error. Furthermore, any CRC error detected increments the FSC Error Counter. To pass payloads without checking the CRC, set the CRC Check Disable bit.

The value of the CRC Check Disable bit does *not* effect the operation FSC Error Counter. This will allow the user to determine the CRC error rate even when processing bad packets. The FSC Error Counter is reset by the user writing a 0 (zero) to this register.

Promiscuous Mode

Bit 4 of the Ethernet Control Register is used to enable/disable "promiscuous mode." This mode is used to indicate whether the MAC source address should be compared against up to 16 possible sources before allowing the data to pass through. By default, this mode is enabled, allowing the Ethernet Filter to capture all frames without discrimination on the Address Compare.

Packet Length Filtering

Packet length filtering can be used to ignore extraneous packets generated by other devices on the network that are not intended to be recorded. This might include ARP requests or other network management requests. Packet length filtering is also part of the Ethernet filter and is bypassed when operating in "Raw" mode. The length filtering is enabled when bit 31 is set in the register. Bits 0-15 are used to define the expected length of the packets to be recorded. This length is the "MAC Client Data" portion of the packet and does not include the preamble, MAC Client Header or FCS blocks.

Data Payload Offset

The Data Payload Offset register is used to define an offset that should be skipped before starting to record data within a packet. When attempting to record "Raw" packets this value should generally be 0 (zero) since it is not disabled by any other filter controls. This value is used to skip data at the beginning of the "MAC Client Data" in each packet. It can be used to avoid recording any OSI network data or other "header" data in the packet. Note that this value can be any number of bytes but the resultant data remaining in the packet to be recorded should always be 8 byte aligned.

Resetting the Ethernet Total Packets Counter

Regardless of the mode, the Ethernet Total Packets counter will count the number of Ethernet Packets processed by the filter without regard to errors or filtering. This counter can be reset by the user by writing a 0 (zero) to this register.

Ethernet Source Address Filter

The Ethernet Filter also has the ability to discriminate based on the Source MAC Address for up to 16 discrete sources. Each source address is made up of two 32 bit registers. One register holds the 4 least significant bytes of the source address and the second register holds the most significant 2 bytes of the source address and an enable bit. The "promiscuous" enable setting overrides these source address comparisons.

10GigE Register Descriptions

Table 3 describes the 10GigE registers.

Register Address	Description
SS_10GIGE_REG_WRAP (0x1)	Read-write register to validate path
SS_10GIGE_REG_DATA_PAYLD_OFFSET (0x3)	The value of the DPOFST (Data Payload Offset)
SS_10GIGE_REG_PSN_OFFSET (0x5)	The value of PSN Offset
SS_10GIGE_REG_FILL_PATTERN (0x7)	Skipped Payload fill Patterns.
SS_10GIGE_REG_TOTAL_PKTS (0x8)	Status Register indicating the total number of packets transmitted.
SS_10GIGE_REG_NUM_ERR_PKTS (0x9)	Status Register indicating the total number of packets which have length error.
SS_10GIGE_REG_ETHR_FILTER_CTRL (0xC)	Ethernet Filter Specific Control Bit 4 (0x00000010) – Enable promiscuous mode, disable source address comparison. Enabled by default at reset. Bit 2 (0x00000004) – CRC Check Disable Bit 0 (0x00000001) – Disable all filtering (Raw mode)
SS_10GIGE_REG_ETHR_PKT_LENGTH (0xD)	Ethernet Filter Specific Packet length Bit 31 (0x80000000) – Enable packet length filtering. Bits 15:0 (0x0000XXXX) – Expected packet length.
SS_10GIGE_REG_ETHR_TOTAL_PKTS (0xE)	Ethernet Status Register indicating the total number of packets transmitted.
SS_10GIGE_REG_ETHR_FSC_ERR_PKTS (0xF)	Ethernet Status Register indicating the total number of packets with FSC Ethernet Errors.
SS_10GIGE_REG_ETHR_LGTH_ERR_PKTS (0x10)	Ethernet Status Register indicating the total number of packets with Length Errors.
SS_10GIGE_REG_ETHR_ADDR_RJT_PKTS (0x11)	Ethernet Status Register indicating the total number of packets rejected because of the address filter.
SS_10GIGE_REG_SRC_ADDR_0_LSB (0x12)	LSB Source Address Compare 0 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_0_MSB (0x13)	MSB Source Address Compare 0 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_1_LSB (0x14)	LSB Source Address Compare 1 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_1_MSB (0x15)	MSB Source Address Compare 1 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_2_LSB (0x16)	LSB Source Address Compare 2 Bits 31:0 – Source MAC address bytes 4:0

SS_10GIGE_REG_SRC_ADDR_2_MSB (0x17)	MSB Source Address Compare 2 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_3_LSB (0x18)	LSB Source Address Compare 3 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_3_MSB (0x19)	MSB Source Address Compare 3 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_4_LSB (0x1A)	LSB Source Address Compare 4 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_4_MSB (0x1B)	MSB Source Address Compare 4 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_5_LSB (0x1C)	LSB Source Address Compare 5 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_5_MSB (0x1D)	MSB Source Address Compare 5 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_6_LSB (0x1E)	LSB Source Address Compare 6 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_6_MSB (0x1F)	MSB Source Address Compare 6 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_7_LSB (0x20)	LSB Source Address Compare 7 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_7_MSB (0x21)	MSB Source Address Compare 7 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_8_LSB (0x22)	LSB Source Address Compare 8 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_8_MSB (0x23)	MSB Source Address Compare 8 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_9_LSB (0x24)	LSB Source Address Compare 9 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_9_MSB (0x25)	MSB Source Address Compare 9 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5

SS_10GIGE_REG_SRC_ADDR_A_LSB (0x26)	LSB Source Address Compare 10 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_A_MSB (0x27)	MSB Source Address Compare 10 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_B_LSB (0x28)	LSB Source Address Compare 11 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_B_MSB (0x29)	MSB Source Address Compare 11 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_C_LSB (0x2A)	LSB Source Address Compare 12 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_C_MSB (0x2B)	MSB Source Address Compare 12 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_D_LSB (0x2C)	LSB Source Address Compare 13 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_D_MSB (0x2D)	MSB Source Address Compare 13 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_E_LSB (0x2E)	LSB Source Address Compare 14 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_E_MSB (0x2F)	MSB Source Address Compare 14 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5
SS_10GIGE_REG_SRC_ADDR_F_LSB (0x30)	LSB Source Address Compare 15 Bits 31:0 – Source MAC address bytes 4:0
SS_10GIGE_REG_SRC_ADDR_F_MSB (0x31)	MSB Source Address Compare 15 Bit 31 (0x80000000) – Enable this source address compare Bits 16:0 – Source MAC address bytes 6:5

CE Mark Declaration of Conformity

CE Declaration of Conformity

CONDUANT

(Manufacturer)	Conduant Corporation
(Address)	1501 South Sunset Street, Suite C
	Longmont, CO 80501 USA

declares that the product:

Mezzanine I/O Board, model StreamStor Copper High Speed Serial Mezzanine Board, for use with StreamStor PCI based controller cards such as the Amazon, electrical supply input rated 3.3Vdc 2A.

conforms to the following Directives:

1. Low Voltage Directive 2006/95/EC
2. Electromagnetic Compatibility Directive 2004/108/EC

using the following primary standards:

EN 60950-1 2nd Edition : Safety of Electrical Equipment for Information Technology Equipment

EN 55024: 2010 : Immunity Standard for Information Technology Equipment

EMC Requirements:

EN 55022: 2006 +A1 :2007	: Radiated and Conducted Emissions - Class A
EN 61000-4-2	: Electrostatic Discharge
EN 61000-4-3	: Radiated RF Immunity
EN 61000-4-4	: Electrical Fast Transients/Burst
EN 61000-4-5	: Surge Immunity
EN 61000-4-6	: Conducted RF Immunity
EN 61000-4-8	: Power Frequency H Field Immunity
EN 61000-4-11	: Voltage Dips, Interruptions
EN 61000-3-2	: AC Harmonic Emissions
EN 61000-3-3	: AC Short and Long Term Flicker

and complies with the relevant Essential Health and Safety Requirements.

I, undersigned, hereby declare that the equipment specified above conforms to the above Directives and Standards and is therefore eligible to carry the CE Marking.

Ken Owens	President/CEO	Ken Owens
(Name)	(Position)	(Signature)

Longmont, Colorado — September 14, 2011 (Date)

Technical Support

Conduant wants to be sure that your StreamStor system works correctly and stays working correctly. In the event, however, that you are unable to get your system to work properly, or if a working system ceases to function, we will do all that we can to get your system back online.

Solving the problem is largely a matter of data collection and steps that must be taken one at a time. In order for us to better serve you, we ask that you take the time to perform the following steps prior to calling us. This way, you can provide us with the most meaningful information possible that will help us solve the problem.

Is the problem one that obviously requires replacement parts due to physical damage to the system? If yes, then please gather the information described below and report the problem to tech support, by phone or through the Conduant web site.

Have you confirmed that no cabling has been inadvertently disconnected or damaged while working around the equipment?

Is the StreamStor card properly seated in the PCI (CPCI/PXI) slot?

Do all the systems have good power connections and voltages?

Does the confidence test sscfg.exe (on Windows) or ssopen/sstest (on Linux) run OK?

Has the software installation been corrupted? Try re-installing software.

Have you checked the Conduant web site for technical bulletins?

Have you recently installed a new Linux kernel or compiler or a new Windows Service Pack?

If the above steps did not resolve the problem, then please initiate a trouble ticket on the support section of the Conduant website at www.conduant.com. Please provide as much information about your system and the problem as possible. We will do all that we can to resolve the problem as quickly as possible.